PTO/SB/08B (04-03)

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Substitute for form 1449/PTO	Complete if Known		
Substitute for form 1449/1 TO	Application Number		
INFORMATION DISCLOSURE	Filing Date	June 28, 2003	
STATEMENT BY APPLICANT	First Named Inventor	Chih-Hsin Wang	
	Art Unit		
(Use as many sheets as necessary)	Examiner Name		
Sheet 1 of 1	Attorney Docket Number		

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Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
		Kitamura et al., "A Low Voltage Operating Flash Cell with High Coupling Ratio Using Horned Floating Gate with Fine HSQ," Symposium on VLSI Technology, P.104, 1998				
		Lai, "Flash Memories: Where We Were and Where We Are Going", IEDM Technical Digest, pp.971-973, 1998.				
		Kuo et al., "TEFET – A High Density, Low Erase Voltage, Trench Flash EEPROM", Symposium on VLSI Technology, P.らり、1994				
		Wang et al, "Three-Dimensional DIBL for Shallow-Trench Isolated MOSFET's", IEEE Trans. on Electron Devices, مام دور المراجعة الم				
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INFORMATION DISCLOSURE	Filing Date	June 28, 2003		
INFORMATION DISCLOSURE	First Named Inventor	Chih-Hsin Wang		
STATEMENT BY APPLICANT	Art Unit			
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haat 11	Attorney Docket Number			

			U. S. PATEN	T DOCUMENTS	
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ^{2 (f known)}	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		^{US-} 5,780,341	07-14-1998	Seiki Ogura	Figs.4A,4B,6A,6B
		US-			Fig. 7A
		^{US-} 4,957,877	09-18-1990	Simon M. Tam et al.	Figs. 5A, 5B
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		^{US-} 6,479,863 B2	11-12-2002	John Caywood	Figs, 3b, 5b, 17d,
		US-	1 - 1 - 1 - 1 - 1	The state of the s	17e,18d
		^{US-} 6,372,617 B1	04-16-2002	T. Kitamura	Fig. 3A
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FOREIGN PATENT DOCUMENTS								
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